

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of active pixel type photoreceptors, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and further comprising double sampling charge storage elements on said substrate.

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26. (Amended) A single chip camera device,
comprising:

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CND
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which

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are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

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cont
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors,

wherein said timing circuit allows changing an integration time for said array of photoreceptors.

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(Amended) A single chip camera device, comprising:

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cont
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

C4 Contd
said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, in a way such that a least a plurality of said photoreceptors output their signals at substantially the same time,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

35. (Amended) A single chip camera device, comprising:

C5 Contd
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said

photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

C5 cont
said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said array of photoreceptors includes an active pixel sensor, where each element of the array includes both a photoreceptor and a readout amplifier integrated within the same substrate as the photoreceptor.

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N* (Amended) A single chip camera device, comprising:

C6 Cont
a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a

preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

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~~44~~ (Amended) A single chip camera device,
comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

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cont.

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, and a noise reduction circuit.

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N (Amended) A single chip camera device, comprising:

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cont.

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors in a first mode or in a second mode, depending on a type of photoreceptor being used,

c7 could

further comprising a noise reduction circuit.

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98. (Amended) A single chip camera device,
comprising:

a substrate, having integrated thereon an image
acquisition portion and a control portion, both of which
are formed using a logic family that is compatible with
CMOS;

said image acquisition portion integrated in said
substrate including an array of photoreceptors;

08 said control portion integrated in said substrate
including a signal controlling device, controlling said
photoreceptors to output their signals,

said control portion also including, integrated in
said substrate, a timing circuit integrated within the same
substrate that houses the array of photoreceptors,
controlling a timing of operation of said array of
photoreceptors,

said control portion including common logic elements
to control row and address decoders and delay counters,
further comprising a mode selector device, selecting a mode
of operation of said chip.

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101. (Amended) A single chip camera device,
comprising:

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

C9. said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.

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Cmt
113. (Amended) A single chip camera device,
comprising;

a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition integrated in said substrate including an array of photoreceptors arranged in rows and columns;

a charge storage element, associated with each said column;

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CP said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals,

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors;

said control portion including common logic elements to control all pixels on a selected row to sample said all pixels onto said charge storage elements substantially simultaneously, further comprising a mode selector device, selecting a mode of operation of said chip.

65 117. (Amended) A single chip camera device,
comprising:

CM a substrate, having integrated thereon an image acquisition portion and a control portion, both of which are formed using a logic family that is compatible with CMOS;

said image acquisition portion integrated in said substrate including an array of photoreceptors;

said control portion integrated in said substrate including a signal controlling device, controlling said photoreceptors to output their signals, and including a preset buffer, allowing preset of at least one of a start address for output or a stop address for output;

said control portion also including, integrated in said substrate, a timing circuit integrated within the same substrate that houses the array of photoreceptors, controlling a timing of operation of said array of photoreceptors, wherein said timing circuit allows changing an integration time for said array of photoreceptors.